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| Form PTO-100 (Modified)                  | Atty Docket No.<br>42390P11927            | RECEIVED<br>Application No.<br>10/037,666     |
| List of Patents & Publications Statement | Applicant(s):<br>Sriram Vajapeyam, et al. | APR - 9 2002<br>TECHNOL<br>Group No.:<br>2800 |
| (Use several sheets if necessary)        | Filing Date:<br>January 03, 2002          | Group No.:<br>2819                            |

# U.S. PATENT DOCUMENTS

| Exam. Initials |    | Document Number | Date       | Name                | Class | Sub-class | Filing Date (if appropriate) |
|----------------|----|-----------------|------------|---------------------|-------|-----------|------------------------------|
| DJH            | AA | 5,699,537       | 12/16/1997 | Sharangpani, et al. |       |           |                              |
|                | AB |                 |            |                     |       |           |                              |
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# FOREIGN PATENT DOCUMENTS

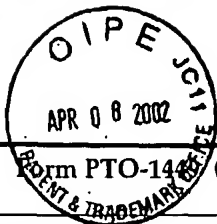
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# OTHER ART (Including Title, Author, Date, Pertinent Pages, etc.)

| Exam. Initials |    | Document Identification   |
|----------------|----|---|
| DJH            | AR | Yuan Chou, John Shen, "Instruction Path Coprocessors", In Proceedings of 27th Annual International Symposium on Computer Architecture, pgs. 270-281, June 2000.           |
| DJH            | AS | R. Iannucci, "Toward a Dataflow/von Neumann Hybrid Architecture", In Proceedings of 15th International Symposium on Computer Architecture, pgs. 131-140, 1988.            |
| DJH            | AT | S. Palacharla, James Smith, "Complexity-Effective Superscalar Processors", In 24th International Symposium on Computer Architecture, pgs. 206-218, Denver, CO, June 1997. |

Examiner: David J. Shuman Date Considered: 8-3-04

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication



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|--|--|---------------------------------|
| Form PTO-1446 (Modified)                 | Atty Docket No.<br>42390.P11927                        | Application No.<br>RE10,017,666 |
| List of Patents & Publications Statement | Applicant(s):<br>Sriram Vajapeyam, et al. APR - 9 2002 |                                 |
| (Use several sheets if necessary)        | Filing Date:<br>January 3, 2002                        | Group No.:<br>2819              |

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#### OTHER ART (Including Title, Author, Date, Pertinent Pages, etc.)

| Exam. Initials |    | Document Identification  |
|----------------|----|--|
| 0JH            | AR | J.E. Smith, "Instruction-Level Distributed Processing," IEEE Computer, April 2001.   |
| 0JH            | AS | Sriram Vajapeyam, Tulika Mitra, "Improving Superscalar Instruction Dispatch and Issue by Exploiting Dynamic Code Sequences," 7th International Symposium on Computer Architecture, India, December 1997. |
|                | AT |  |

Examiner: David J. Hummer Date Considered: 8-3-07

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| Form PTO-1449 (Modified)                 | Atty Docket No.<br>42390P11927            | Application No.<br>10/037,666 |
| List of Patents & Publications Statement | Applicant(s):<br>Sriram Vajapeyam, et al. | APR -9 2002                   |
| (Use several sheets if necessary)        | Filing Date:<br>January 03, 2002          | Group No.:<br>2819            |

## U.S. PATENT DOCUMENTS

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## OTHER ART (Including Title, Author, Date, Pertinent Pages, etc.)

| Exam. Initials |    | Document Identification  |
|----------------|----|--|
| 0074           | AR | Sanjay J. Patel, Steven S. Lumetta, "rePLay: A Hardware Framework for Dynamic program Optimization." Tech. Rep. CRHC-99-16, Center for Reliable High-Performance Computing, Univ. Illinois, Dec. 1999.                                 |
| 0074           | AS | Narayan Ranganathan, Manoj Franklin, "An Empirical Study of Decentralized ILP Execution Models," In 8th International Conference on Architectural Support for Programming Languages and Operation Systems, pgs. 271-281, October 1998. |
| 0074           | AT | Narayan Ranganathan, Manoj Franklin, "The PEWs Microarchitecture: Reducing Complexity Through Data-Dependence Based Decentralization," Microprocessor and Microprocessing Systems, 1998.   |

Examiner: David J. Kuni Date Considered: 6-3-04

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| Form PTO-1449 (Modified)                 | Atty Docket No.<br>42390.P11927           | Application No.<br>10/037,666 |
| List of Patents & Publications Statement | Applicant(s):<br>Sriram Vajapeyam, et al. |                               |
| (Use several sheets if necessary)        | Filing Date:<br>January 3, 2002           | Group No.:<br>2819            |

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OTHER ART (Including Title, Author, Date, Pertinent Pages, etc.)

| Exam. Initials |    | Document Identification   |
|----------------|----|---|
| 034            | AR | Eric Rotenberg, Steve Bennett, James E. Smith, "A Trace Cache Microarchitecture and Evaluation", IEEE Transactions on Computers, 48(2): 111-120 (1998). |
| 034            | AS | Eric Rotenberg, "Trace Processors: Exploiting Hierarchy and Speculation". Ph.D. Thesis, Computer Sciences Dept. Univ. of Wisconsin - Madison (1996).    |
|                | AT |   |

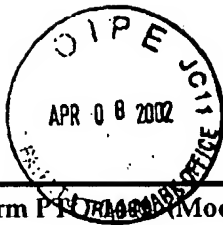
Examiner:

*David J. Thum*

Date Considered:

8-3-04

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| Form PTO 700 (Modified)                  | Atty Docket No.<br>42390.P11927           | Application No.<br>40/037,666 |
| List of Patents & Publications Statement | Applicant(s):<br>Sriram Vajapeyam, et al. |                               |
| (Use several sheets if necessary)        | Filing Date:<br>January 3, 2002           | Group No.:<br>2819            |

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| Exam. Initials |    | Document Identification   |
|----------------|----|---|
| 034            | AR | Sanjay J. Patel, Tony Tung, Satarupa Boe, Matthew M. Crum, "Increasing the Size of Atomic Instruction Blocks Using Control Flow Assertions," Proceedings of 33rd Annual International Symposium on MicroArchitecture, 2000. |
| 034            | AS | Amir Roth, Guri Sohi, "Speculative Data-Driven Sequencing for imperative Programs," UW-Madison TechReport, March 2000.  |
| 034            | AT | J.E. Smith, "Instruction-Level Distributed Processing," Proc. Int'l. Symp. on High-Performance Computing, Dec. 2000.  |

Examiner: David J. WhinnDate Considered: 8-3-04

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